

Abstract of the Disclosure

A circuit simulator simulates a circuit described by a circuit logic model as having a set of clocked registers interconnected by un-clocked logic to produce waveform data indicating states of each circuit input signal and of each register output signal as functions of clock signal edge timing. The waveform data and the logic model are then processed to produce a temporal schema model characterizing the circuit's logic and behavior. A display based on the temporal schema model depicts circuit behavior using separate symbols to represent successive circuit input signal states and register output signal states at various times during the simulation. The same display also graphically depicts fan-in or fan-out logical relationships by which circuit input signal states and register output signal states influence register input signal states.

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